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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,223	08/17/2001	William J. Mitchem	McD121	4892

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EXAMINER	
PARK, JUNG H	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,223	MITCHEM, WILLIAM J.	
	Examiner	Art Unit	
	Jung Park	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-18* is/are allowed.

6)☒ Claim(s) *19-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/03/01* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-42 are pending for the examination.

Drawings

2. The drawings are objected to because:

In Figure 2, the "Tx Module" 220 should be changed to -- Rx Module -- since there is no Rx module in the GL Port 1.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities:

There are no brief descriptions for figure 4A and 4B (see page 4).

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 19-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paul et al. (U.S. Pub. No. 2005/0047334; hereafter "Paul") and further in view of Martin et al. (U.S. Pub. No. 2002/0167958; hereafter "Martin").

Paul's disclosure is related to a Fibre Channel switch having the ability to track congested ports, manage flow control over virtual channels on an inter-switch link and shows all the elements of a Fibre Channel switch in his drawings.

Martin's disclosure is related to a system and method for storing and retrieving multi-speed data streams with a network switch.

As to claim 19, Paul teaches a fibre channel fabric (200 Fig. 4) comprising: a fibre channel switch (100 Fig. 1) having a plurality of fibre channel ports (110 Fig. 1) embodied thereon for transmitting and receiving data frames (114 Fig. 1 and 112 Fig. 1; col. 5, para. 73; col. 5, para. 74);

a route control module (330 Fig. 2) coupled to one of plurality of fibre channel ports, route control module for providing an exit port (col. 6, para. 85) in response to a request from plurality of fibre channel ports for exit port, request comprising a destination identification (col. 6, para. 85); and

a memory location (340 and 350 Fig. 3), memory location coupled to each of plurality of fibre channel ports (110 and 310 Fig. 3), wherein memory location stores data frames (col. 5, para. 73) transmitted to each of plurality of fibre channel ports (col. 5, para. 73), wherein fibre channel switch has more than one rate for reading and writing data memory location (*reading and writing module,* col. 6, para. 86) to each of plurality of fibre channel ports.

Although Paul teaches the method of reading and writing of data frame from memory buffer to fibre channel ports, Paul is silent on the different reading and writing rates from/to memory. However, Martin discloses a *central (shared) memory architecture, within the switch, which is capable of writing and reading data to the memory at different speeds* (col. 2, para. 13). Therefore, it would be obvious for one of ordinary skill in the art to combine the feature in Martin with Paul for the purpose of using different reading and writing rates in the shared memory. The motivation would be to adopt different reading/writing speeds of memory to the switching system to reduce the memory waste.

6. As to claim 20, Paul teaches the fibre channel fabric further comprising an interface control module (*packet processing unit,* col. 2, para. 15) that couples a first fibre channel

port and a second fibre channel port of fibre channel switch (col. 2, para. 16), where interface control module provides a first control signal (*request signal,* col. 2 para. 15) to second fibre channel switch in response to a second control signal (*acknowledge signal,* col. 2, para. 15) from first fibre channel switch.

7. As to claim 21, it is rejected for the similar reasons set forth in the rejection of claim 19.

8. As to claim 22, Paul teaches memory that comprises a plurality of RAM modules (col. 5, para. 70), but he is silent about using SRAM in the memory. Using SRAM for the shared memory is one to design choice. Hence, it would have been obvious to combine this design choice with Paul for the purpose of simply using static RAM for the shared memory in the switch. Therefore, it would be obvious for one of ordinary skill in the art to combine this design choice with Paul for the purpose of using SRAM for the shared memory. The motivation is to use static RAM for holding its data without external refresh, for as long as power is supplied to the circuit.

9. As to claims 23, it is rejected for the similar reasons set forth in the rejection of claim 22.

10. As to claims 24-25, this is a method for providing a shared memory location at different rates for reading/writing data from/to memory and then gives an example for different speeds. Paul fails to teach a method of providing a shared memory location at different rates and gives an example. However, Martin teaches the memory supporting both 1

Gbps and 2 Gbps read and write date rates (col. 5, para. 54). Also, he teaches the central memory architecture being capable of writing and reading data to the memory at different speeds (col. 2, para. 13) and then shows an example of reading/writing data from/to memory at different speeds (col. 5, para. 53, 55, and 56). It would have been obvious for one of ordinary skill in the art to combine the feature in Martin with Paul for the purpose of using different data reading/writing rates in the memory. The motivation would be to adopt different reading/writing speeds of memory to the switching system to reduce the memory waste.

11. As to claim 26, Paul teaches a bus (150 and 160 Fig. 1) coupled one of plurality of fibre channel ports (*ports0-3* 110 Fig. 1) to a memory (180 Fig. 1).

12. Claims 27, 29 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paul.

As to claims 27 and 35, Paul teaches a method of providing a plurality of first-in first-out (FIFO) data storage locations (444 and 446, Fig. 12), wherein portion of data frame is stored in data storage location before being read to second port (col. 2, para. 12; col. 5, para. 73).

Paul is silent on a method for providing a plurality of columns of memory comprising a plurality of rows for storing a portion of data frames. However, it is well known in the art that a pointer is a memory cell containing the address of another

memory cell by providing a position of column and row. The motivation is to provide simple reading/writing processes by using two dimensional address formats.

As to claim 29, Paul is silent on writing a first port of data frame to a column of memory. However, it is well known in the art that is just a head of data frame. Hence, it would have been obvious to one of ordinary skill in the art at the time of the invention writing the first portion of data frame to the first column of memory. The motivation is to simplify the order of data frames during the writing process.

13. As to claim 28, Paul fails to teach explicitly the number of columns of memory which is equal to or greater than the number of ports. However, it is well known in the art that the number of columns of memory should be equal to or greater than ports in order for fibre channel ports to access a plurality of columns. The motivation is to provide sufficient memory space to avoid overflow of data in the memory.

14. As to claims 30 and 31, Paul is silent on the first portion of frame comprises a word and the word is 34 bits in length, but it is well known in the art that the word is a header or a payload and the length of bits depends on protocols.

15. As to claim 32, Paul is silent on the different reading and writing rates from/to memory. However, Martin discloses a *central (shared) memory architecture, within the switch, which is capable of writing and reading data to the memory at different speeds* (col. 2, para. 13). Therefore, it would be obvious for one of ordinary skill in the art to combine

the feature in Martin with Paul for the purpose of using a first data rate for writing data to the first column of memory and a second data rate for reading from the first column. The motivation would be to provide a different read/write methodology depending on the case.

16. As to claim 36, it is rejected for the similar reasons set forth in the rejection of claim 28.

17. As to claim 37, Paul is silent about if the number of memory location is an odd number, but this is one to design choice. It can be either odd or even.

18. As to claims 38-39, Martin discloses the memory locations that are implemented using RAM modules (col. 4, para. 43). The width of memory location is bits, wherein bits are the length of word of data frame (col. 4 para. 43).

19. As to claim 40, it is rejected for the similar reasons set forth in the rejection of claims 37

20. As to claims 41-42, Paul is silent about the claimed mathematical formulas. However, one of ordinary skill in the art at the time of invention would have realized that the depth of a buffer, which is the same as the size of buffer, and the number of rows per frame are determined by the elements described in the claims. Therefore, it would be obvious to include those terms to conclude the size of buffer and the number of rows per frame. The motivation is to simplify the size of buffer by use of frame, port and row elements.

Allowable Subject Matter

21. Claims 1- 9 are allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest a method which includes the step of transmitting a message from first port to second port indicating the position in shared memory location of a data frame. It is noted that the closest prior art, Banks et al. (U.S. 6160813) show a similar method, within the fibre channel switch, capable of generating a message indicating which memory module contains the beginning of the frame and then sends the message to a transmitting port. However, Banks et al. fail to disclose validating the transmission of a message from a port to a port, specifically indicating the position in shared memory location of the data frame.

22. Claims 10- 18 are allowable over the prior art of record since the cited references taken individually or in combination fail to particularly teach or fairly suggest a method which includes the step of transmitting data frame to the second fibre channel port, wherein writing and reading are performed in a manner that is dependent on the relative rates at which frame is received and transmitted. It is noted that the closest prior art, Martin show a similar method, which validates a central memory architecture, within the fibre channel switch, capable of writing and reading data to the memory at different speeds. However, Martin fails to disclose validating the writing and reading performance depending on the rates at which frame is received and transmitted.

Conclusion

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- U.S. Patent (6,240,096) to Book teaches Fibre Channel switch employing distributed queuing.
- U.S. Patent (5535197) to Cotton shows many key components in shared buffer switching module.
- U.S. Patent (6,535,516) to Leu et al. shows all the components in a switch unit.

Contact Information

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung Park whose telephone number is 571-272-8565. The examiner can normally be reached on Mon-Fri during 7:15-4:45.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KENNETH VANDERPUYE
PRIMARY EXAMINER

Jung Park
Patent Examiner
May 26, 2005